Legend:

A1.4

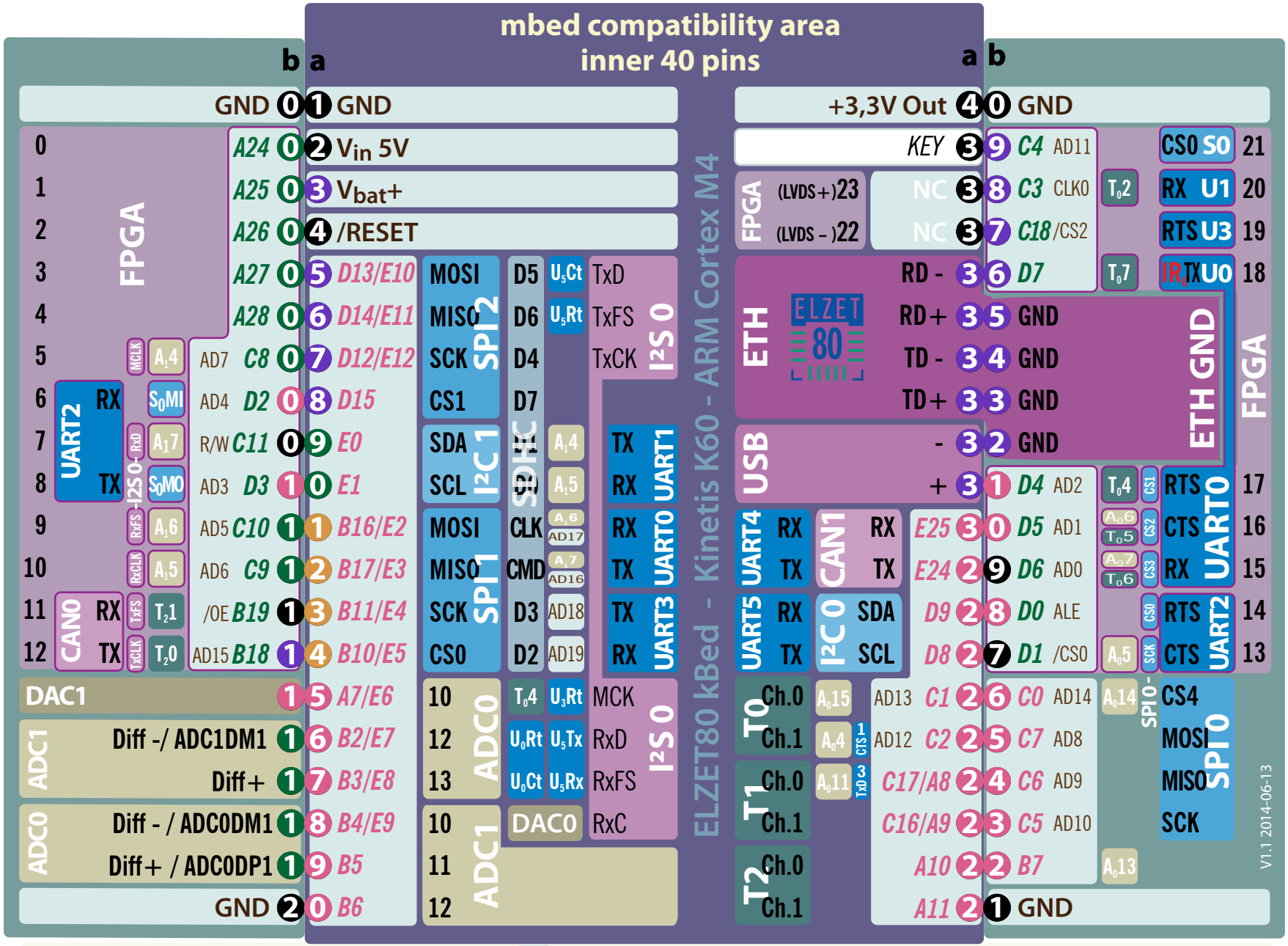
The background color is a hint to the function; here, the beige denotes an analog input.
Areas with a purple outline are available only for the non-FPGA version.

D13/E10

GPIO-Pins. Double designations like above mean that two processor pins are hard wired to one kBed pin (to allow alternate functionality mimicking mBed).

AD19

Possible Flex-bus signals for external i/o or memory. For the FPGA version, an FPGA IP with routed through Flex-bus is available.



Pinout of kBed, not kBed64. Please refer to Excel® sheet for pinout differences