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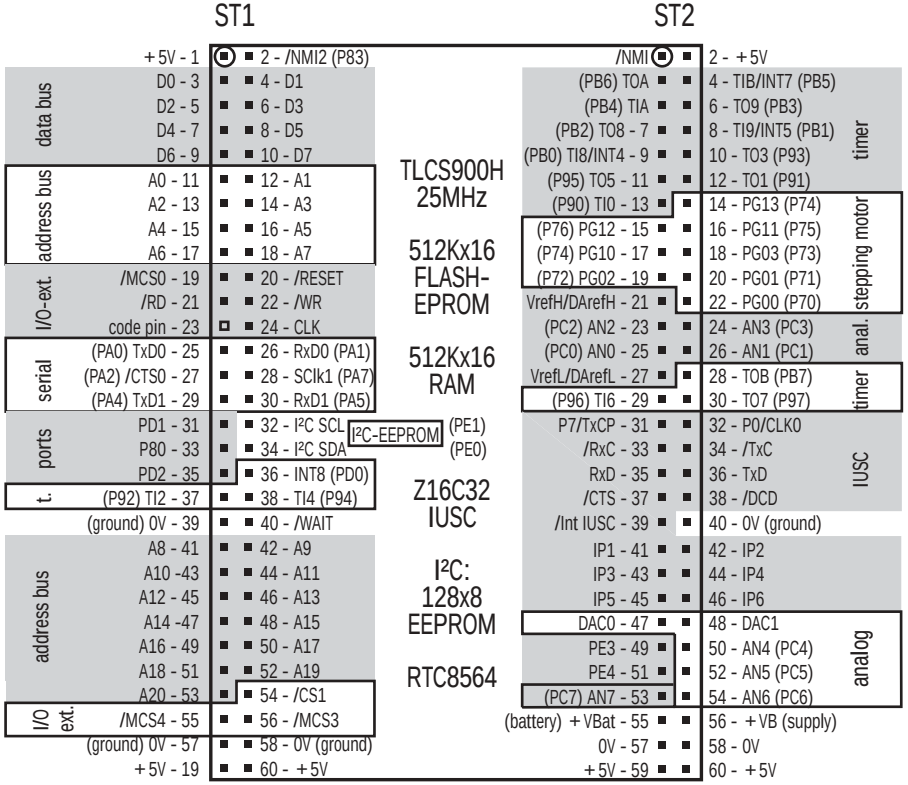
How to install the

V. 1.2 - June02

PER-NET/900H+

processor module



NET/900H+ pin configuration - top view

When installing the module, please make sure to align the pin-1 marks of the module (yellow rings) with the marks on the main board.

Operating the module in the wrong position will damage the module!

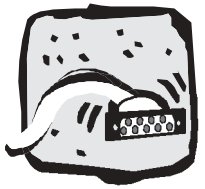
There are no hardware settings to be made at the module. J20 (next to the Li-cell) is only to be closed for access to the bootmonitor - for operating the module with mCAT the jumper has to be left open.

All configuration data is saved in the I²C EEPROM (addr. 1010000b). The addresses from 10h on upwards are available to the user, the area below is used for the operating system data, among others the SerDrv serial interface driver configuration settings..

Access to the EEPROM is gained through mCAT functions, for details see the NVMEM users manual.

RAM, no matter what size, is accessed from address 40 00 00h on. Programs can be loaded into the addresses above 40 20 00 h.

The flash-EEPROM is located at 80 00 00h and



divided into 16 logical pages of 64k. The first three pages are reserved for mCAT. mCAT allows program download into the flash from 80 00 00h on upwards. The default settings for flash and RAM start are to be taken from the target files (.trg). The procedures for downloading are explained in the mCAT users manual.

Usage of I/O connection is dependent on the used main board. The external I/O-pins can be used directly or be extended over the bus. /MCS0 (ST1.19) delivers chip-select for external ports at 4000h..40FFh. For large external areas CS1 is initalized to 10000h-3FFFFFh, however, no more than 2MB are available as only A0..A20 are taken out. Further /MCS3 (C000h-FFFFh) and /MCS4 (1000h..3FFFh) are freely usable.

For information about usage of the internal I/O, the users manual of the TMP95C063 is obligation reading. In reset state, most pins are set to digital input with pull-ups (except for analog input and output-only pins P65..P67). For details see the users manual p. MCU-900-242. Port states are read or written over the port-n-register. The change to output is made with the port-n-control-registers. The port-n-function-registers are used to switch to high-level functions of the port pin, i.e. to timer output or analog input.

The registers are accessible from processor address 0 on. A table of register addresses can be found on page MCU900-409. By inserting the file t95c063.h you can access the register addresses with symbolic names (i.e.: `#define P7CR SFRADDR(byte,0x16)`).

Caution! Many ports are write-only! Their state has to be stored in memory (shadow register) in order to prevent other bits to be changed when one bit is changed.
This is especially critical when ports are used partially by the operating system at P8 and PD. In this case use these settings for your shadow register:

P8R: 1111 1101
P8CR: 0000 0010
P8FC: 0000 0010
PdR: 1111 1111
PdCR: 0000 0000

Serial interfaces

The mCAT-monitor is accessible over the SER0 interface that is also used for program download. The interface doesn't use handshake.

For the usage of SER1 we recommend the module SerDrv, a convenient interface driver.
SerDrv is started automatically with mCAT. Bit rate, etc. are to be configured by function calls and at last the driver for the channel has to be activated by ComOperation call. Until then the hardware can be accessed as usual by polling the registers. After termination of the monitor Ser0 can be used with SerDrv too, but then the processor is not accessible anymore. SerDrv does not support hardware handshake on NET/900H (Integration is available depending on the motherboard).

Used timers

mCAT uses timer T3, if you are going to use T2, make sure not to change the registers T23MOD in the section for T3 - the register is still readable. mCAT might use timer T9 in upcoming versions - please do not use it for your application.

Real time clock

An RTC8564 is attached using the I²C-bus (Adr. 1010001b), access is through mCAT, details are to be found in the Date&Time manual.

I²C

The I²C bus is taken out to ST1, pins 32 (clk) and 34 (data) for external use.

Net/900H is categorically delivered with a runtime license of mCAT2. So you can use all system functions for your application on every module. mCAT is developed furtherly too, so it can happen that you might want to put a new mCAT onto your module.
For this purpose a separate boot monitor *Bootmon* is included, which is located in a protected page in the flash-EPROM but not used for any other purpose. If you want to upgrade to the latest version of mCAT, Bootmon can become active with its communication program.
This allows to load a new mCAT over the serial interface. When trying to do this, you have to close Jumper J2 before switching on the supply voltage - on SER0 you will not get the familiar mCAT message but the Bootmon will come up to provide necessary downloading functions.